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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
NADAV, O	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

1- File Copy

PTO-90C (Rev. 2/95)
*U S GPO 2000-473-000/44602

Application No.	Applicant(s)
09/621,614	Morishita
Examiner	Art Unit
ORI NADAV	2811

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jul 21, 2000 .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-7 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on Jul 21, 2000 is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Drawings

1. Figures 6-7 and 9-15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

2. The disclosure is objected to because of the following informalities: On page 1, line 15, the phrase "or an output terminal" should be omitted. On page 17, line 22, the term "an" should read "a".

Appropriate correction is required.

Claim Objections

3. Claim 4 is objected to because of the following informalities: In line 20, the phrase "region, with a second reference" should read "region is connected with a second". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Watt (5,701,024).

APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section that contains a complementary N type field effect transistor wherein the complementary field effect transistor is composed of a first field effect transistor having a first 3c and second 3b diffusion layers of first conductive type and a gate electrode 6 that is set in the region sandwiched between these layers and a second field effect transistor having a third 4c and fourth 4b diffusion layers of second conductive type and a gate electrode 5 that is set in the region sandwiched between these layers, and a first dopant diffusion region 4a of second conductive type is set at a distance from the region where the first field effect transistor is formed, and a second dopant diffusion region 3a of first conductive type is set at a distance from the region where the second field effect transistor is formed; and the first dopant diffusion region 4a is connected with a first reference potential Vss, the second dopant diffusion

region 3a, with a second reference potential Vdd, and the second diffusion layer 3b and the fourth diffusion layer 4b are each connected with an input/output terminal section 7. APA does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer.

Watt teaches in figure 5 a first conductive type well 54 under the first diffusion layer 44, having a lower dopant concentration than the first diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in order to reduce contact spiking during ESD event.

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of

the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to increase the distance that a spike can propagate without shorting out the junction.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Watt (5,701,024) and Morihisa (JP 10-173070). APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section that contains a complementary N type field effect transistor wherein the complementary field effect transistor is composed of a first field effect transistor having a first 3c and second 3b diffusion layers of first conductive type and a gate electrode 6 that is set in the region sandwiched between these layers and a second field effect transistor having a third 4c and fourth 4b diffusion layers of second conductive type and a gate electrode 5 that is set in the region sandwiched between these layers, and a first dopant diffusion region 4a of second conductive type is set at a distance from the region where the first field effect transistor is formed, and a second dopant diffusion region 3a of first conductive type is set at a distance from the

region where the second field effect transistor is formed; and the first dopant diffusion region 4a is connected with a first reference potential Vss, the second dopant diffusion region 3a, with a second reference potential Vdd, and the second diffusion layer 3b and the fourth diffusion layer 4b are each connected with an input/output terminal section 7.

APA does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer.

Watt teaches in figure 5 a first conductive type well 54 under the first diffusion layer 44, having a lower dopant concentration than the first diffusion layer. Morihisa teaches in figure 2 a first conductive type well 5' under the first diffusion layer 16, wherein the bottom of the first conductive type well 5' is at the same depth as the bottom of the second conductive type well 5 or at a level deeper than the bottom of the second conductive type well, and having a lower dopant concentration than the first diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in order to reduce contact spiking during ESD event.

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to increase the distance that a spike can propagate without shorting out the junction.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-C and N are cited as being related to

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

September 19, 2001